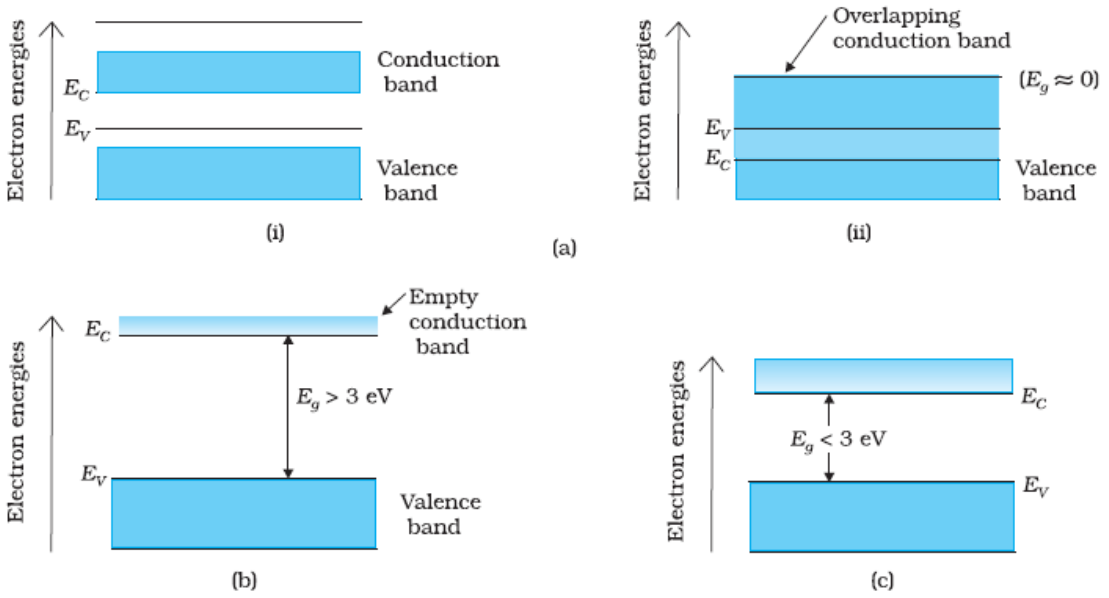


FIGURE 14.2 Difference between energy bands of (a) metals, (b) insulators and (c) semiconductors.

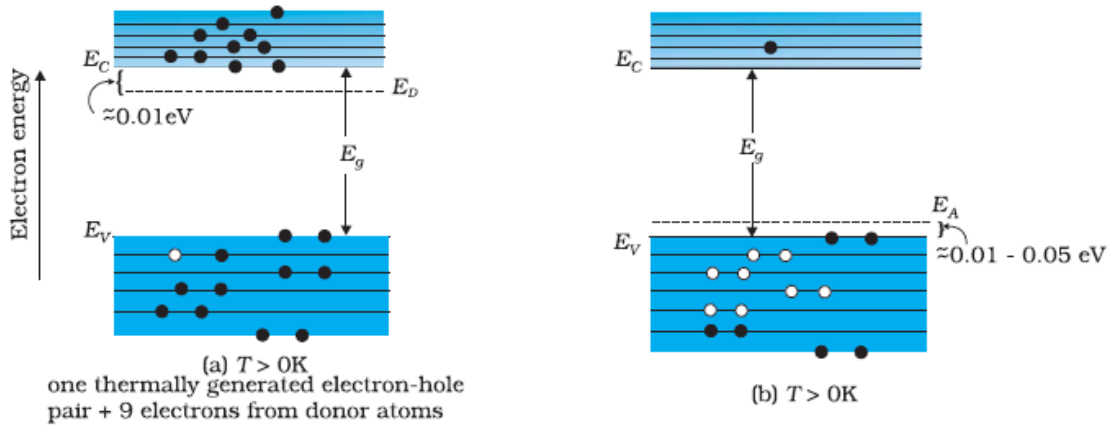


FIGURE 14.9 Energy bands of (a) n-type semiconductor at $T > 0$K, (b) p-type semiconductor at $T > 0$K.

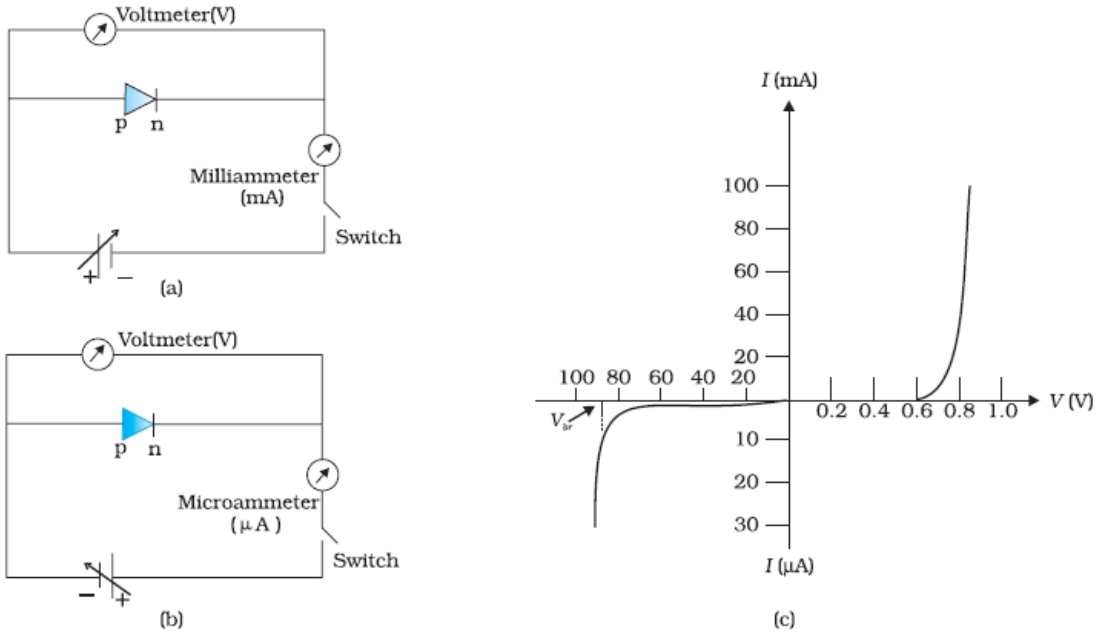


FIGURE 14.16 Experimental circuit arrangement for studying *V-I* characteristics of a p-n junction diode (a) in forward bias , (b) in reverse bias. (c) Typical *V-I* characteristics of a silicon diode.

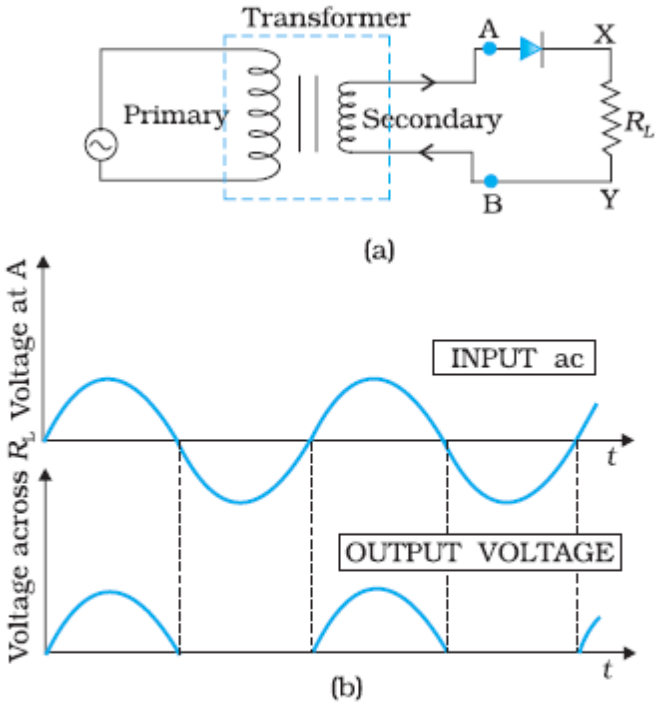


FIGURE 14.18 (a) Half-wave rectifier circuit, (b) Input ac voltage and output voltage waveforms from the rectifier circuit.

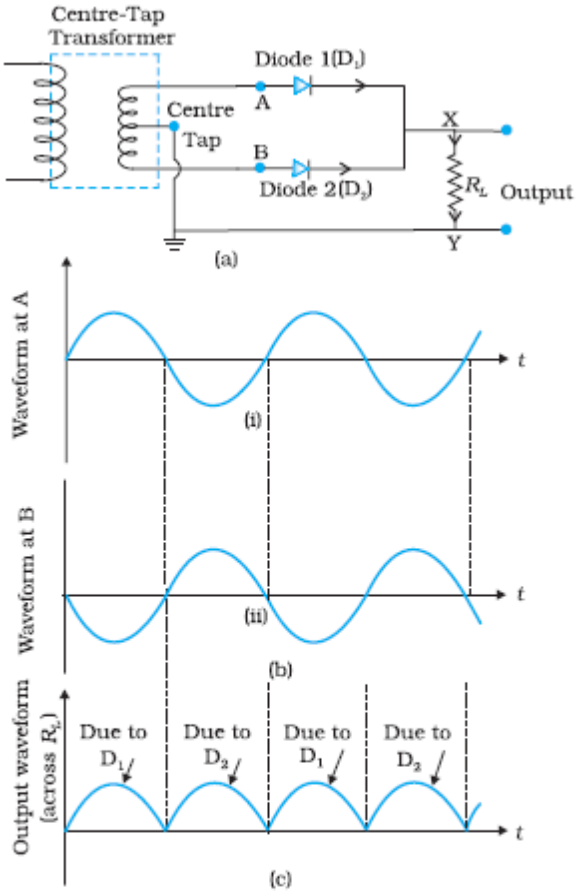


FIGURE 14.19 (a) A Full-wave rectifier circuit; (b) Input wave forms given to the diode D_1 at A and to the diode D_2 at B; (c) Output waveform across the load R_L connected in the full-wave rectifier circuit.

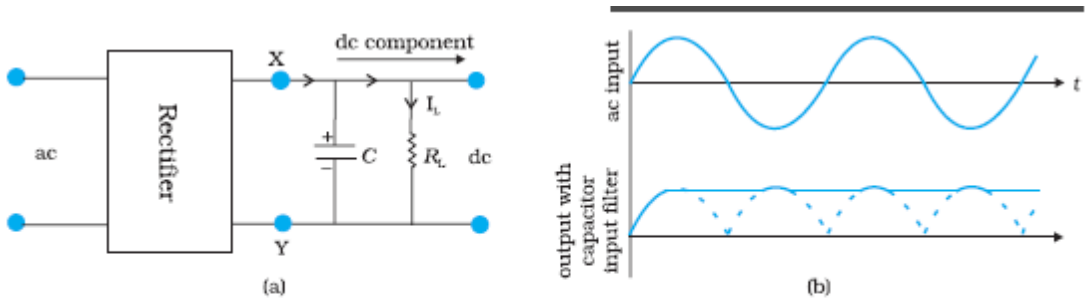


FIGURE 14.20 (a) A full-wave rectifier with capacitor filter, (b) Input and output voltage of rectifier in (a).

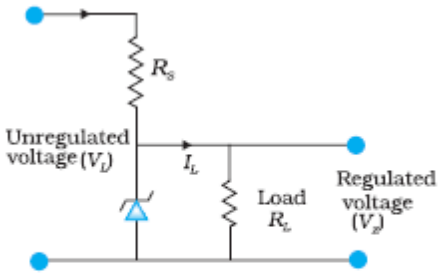


FIGURE 14.22 Zener diode as DC voltage regulator (to be corrected).

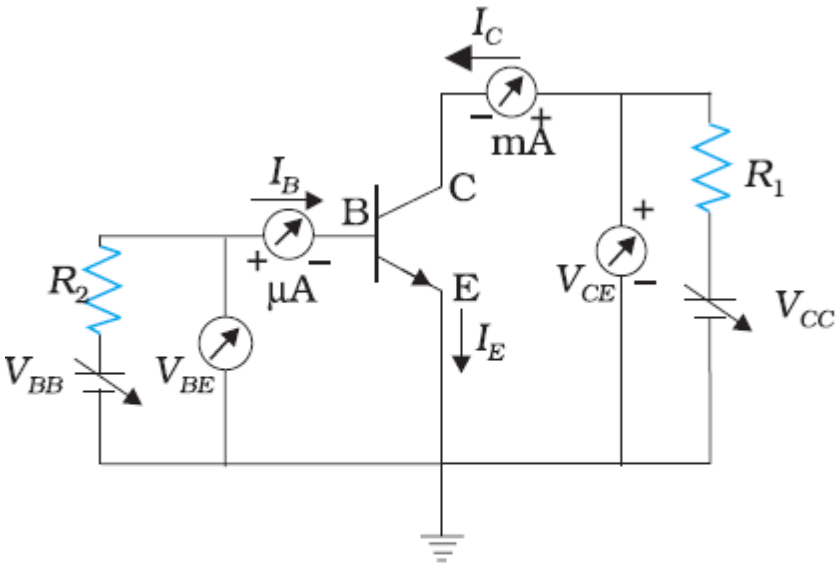


FIGURE 14.29 Circuit arrangement for studying the input and output characteristics of n-p-n transistor in CE configuration.

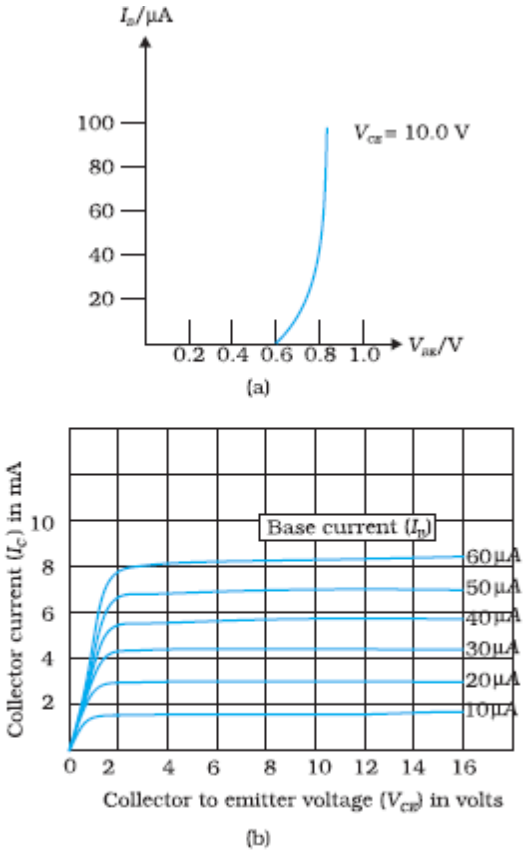


FIGURE 14.30 (a) Typical input characteristics, and (b) Typical output characteristics.

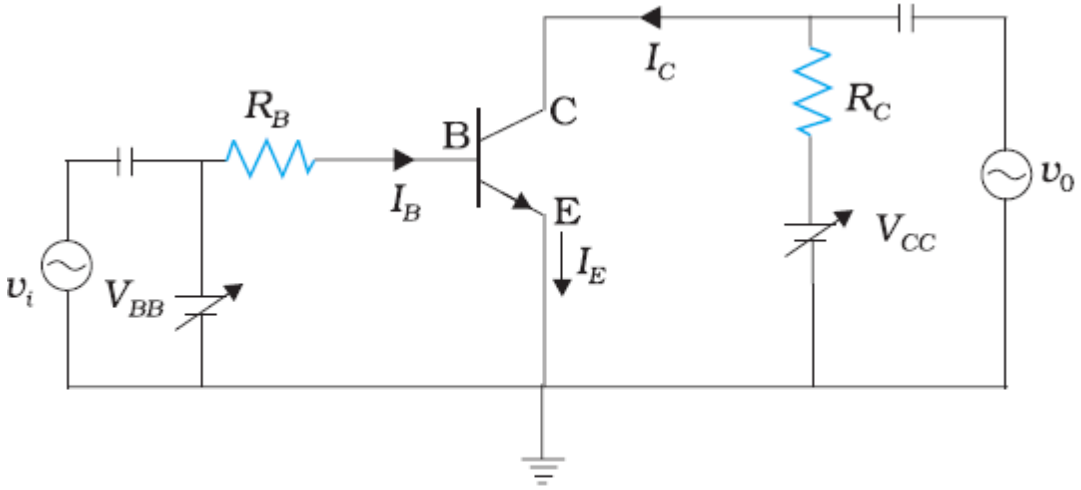
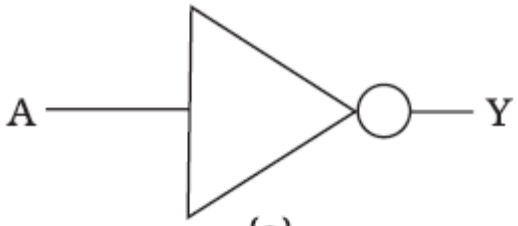


FIGURE 14.32 A simple circuit of a CE-transistor amplifier.

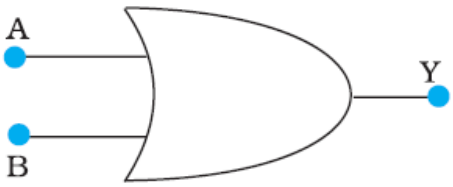


(a)

Input	Output
A	Y
0	1
1	0

(b)

FIGURE 14.35
(a) Logic symbol,
(b) Truth table of
NOT gate.

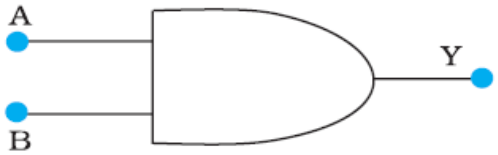


(a)

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b)

FIGURE 14.36 (a) Logic symbol (b) Truth table of OR gate.

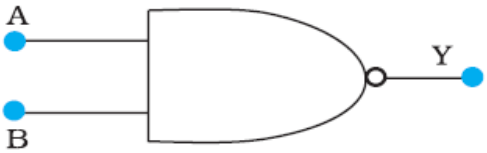


(a)

FIGURE 14.38 (a) Logic symbol, (b) Truth table of AND gate.

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

14.16 and 14.17).

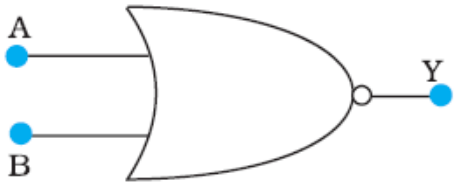


(a)

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(b)

FIGURE 14.40 (a) Logic symbol, (b) Truth table of NAND gate.



(a)

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(b)

FIGURE 14.42 (a) Logic symbol, (b) Truth table of NOR gate.